Amendments to the Specification:

Please replace the paragraph beginning at page 11, line 7, with the following rewritten paragraph:

The outputs of the adders 819 and 821 are then passed to accumulators 833 and 835. If an accumulate operation is not being performed, a zero value is output from multiplexers 829 and 831 to accumulators 833 and 835 to produce a zero input for no accumulation. If an accumulate operation is being performed, the contents of current target registers Rt.H1 and Rt.H1, shown as registers 837 and 839, is output from multiplexers 829 and 831 to accumulators 833 and 835 as an input to produce an accumulated result. Multiplexers 829 and 831 are controlled by an accumulator control signal 841. The outputs of the accumulators [823]833 and [825]835 are then written to the target registers 837 and 839 which contain the 32 bit real result and the 32 bit imaginary result, respectively.

Please replace the paragraph beginning at page 11, line 16, with the following rewritten paragraph:

If an extended precision operation is being performed, the accumulation is augmented eight extra bits by adding the contents of an extended precision registers 843 and 844 to the sign extended output of adders 819 and 821. The outputs of the accumulators 833 and 835 are then written back to the target registers 837 and 839, and the XPR registers 843 and 844, such that registers 843 and [837]847 contain one of the 40 bit results and registers 844 and 839 contain the other 40 bit result. Real and imaginary results are specified by instructions.